Fermilab

SSD Backplane Tests

Prototype Module

Version BP1

February 29, 1990

1. General Information

1.1. Description

This backplane is installed in a FASTBUS crate as defined in IEEE 960. It is a component part of a readout system for Silicon Strip Detectors used in experiments at Fermilab. The crate is populated as shown in Figure 1. The backplane is made in one piece to simplify the assembly of these crates. This will eliminate the requirement for external power connections to the Auxiliary connectors.

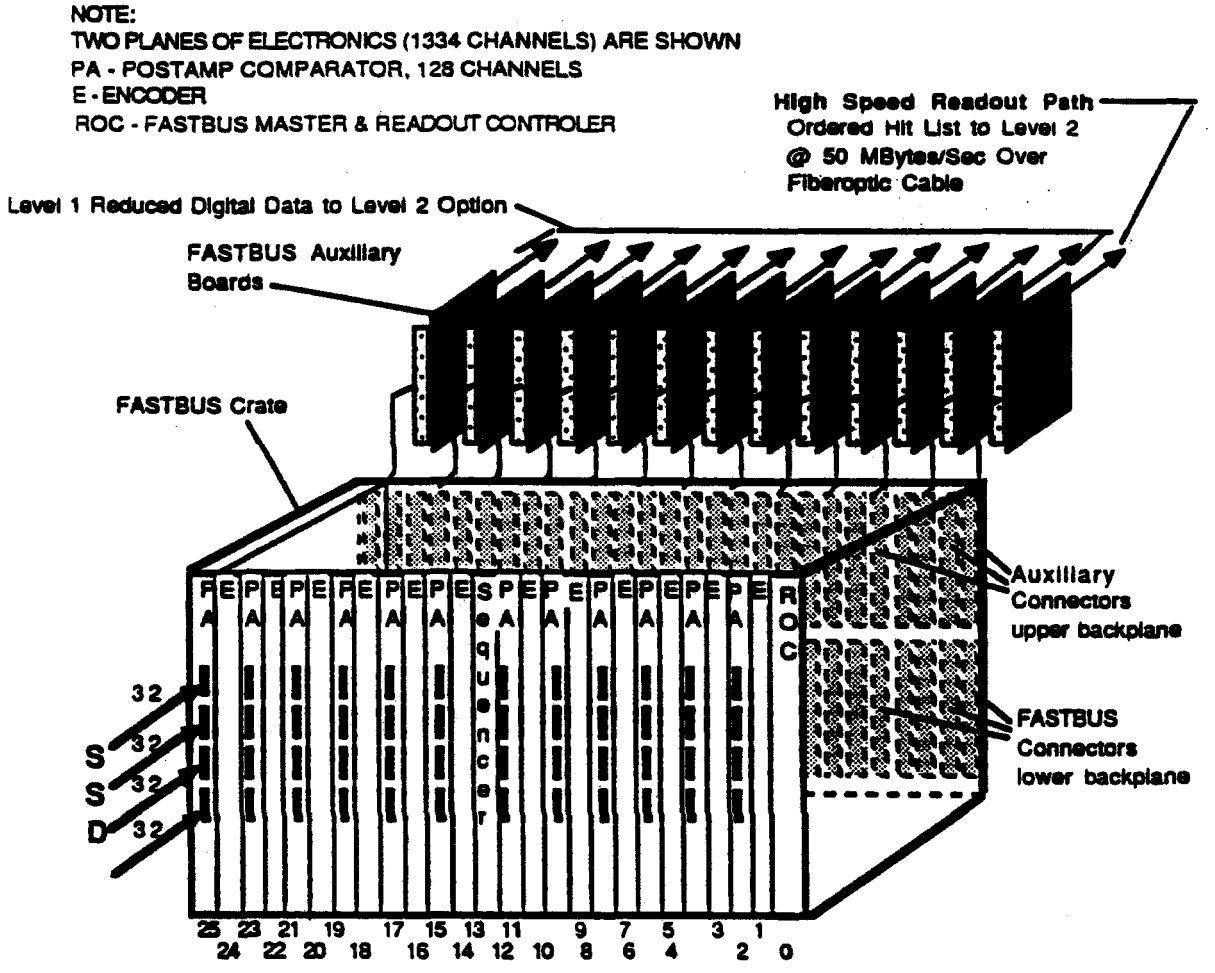

Figure 1

1.2. Specification

The backplane will be constructed of fiber glass reinforced epoxy laminate of type G-10 or FR4. All signal layers are a minimum of .003 inch copper except the Ground, +5.0 Volt and -5.2 Volt layers which are minimum of .004 inch. The thickness of the layers within the lamination must be closely controlled to provide a transmission line environment using stripline and microstrip techniques.

There are two external signal layers, four internal signal layers, three power and three ground layers. The crossection is shown in Figure 2. All signals are normal ECL. Clocks are separated physically by isolation in layers. The signals in these layers are discussed in following sections.

SSD Backplane Crossection

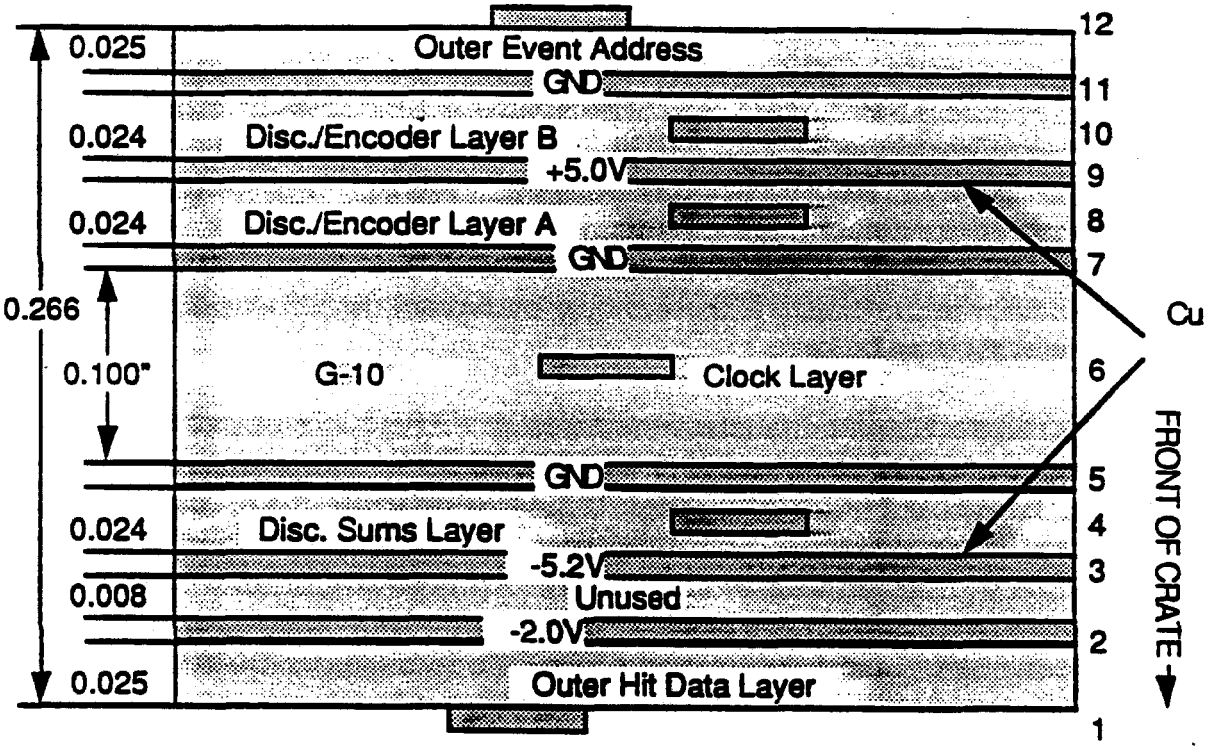

Figure 2

1.3. Test Procedure

The Prototype crates are first sent to Computing Division, Instrument Repair Group for testing of the FASTBUS Segment backplane. The Instrument Repair group has a special test stand for testing the connectivity and mechanical specifications of a FASTBUS crate.

After this is complete a crate will be sent to Kinetic Systems Inc. which has a power distribution test stand for FASTBUS crates. They have agreed to do this part of the testing.

At the same time the Computing Division, Data Acquisition Electronics Department will begin testing the Auxiliary backplane of the other prototype.

2. Mechanical

2.1. Specification

The mechanical dimensions and mounting provisions of the backplane must fit the backplane area of a Kinetics System FASTBUS Crate model # F050-A11. A mechanical drawing of the backplane, showing mounting holes and connector positions, is attached. The lower backplane is detailed in chapter 14 of the FASTBUS specification, IEEE 960. Power connections must conform to the mechanical requirements of the Kinetic Systems Crate named above. This rest of this document refers to the Auxiliary section of the backplane. Where the IEEE 960 Auxiliary backplane specifications differ, this document shall be used.

All Auxiliary backplane connectors are three row 195 pin connectors. The connectors are as specified in chapter 14 of IEEE 960 and figures 14.2 (a & b) of IEEE 960 and addendum's to the specification. The Auxiliary connectors are provided with a shroud/card guide as shown in figure 14.2(c) of IEEE 960 or guide pins as shown in detail A of the supplied mechanical drawing. The connectors have daughter cards on both sides of the Auxiliary backplane. Daughter card connectors will conform to appendix K of IEEE 960. Daughter cards will be plugged into both sides of the backplane.

2.2. Test Procedure

The Instrument Repair Group has a special test stand for FASTBUS crates and test jigs to check dimensional tolerances.

2.3. Test Result

The terminator sips for the Auxiliary backplane interfere with the insertion of modules. Interlogic will Modify crates to place the sips on the back.

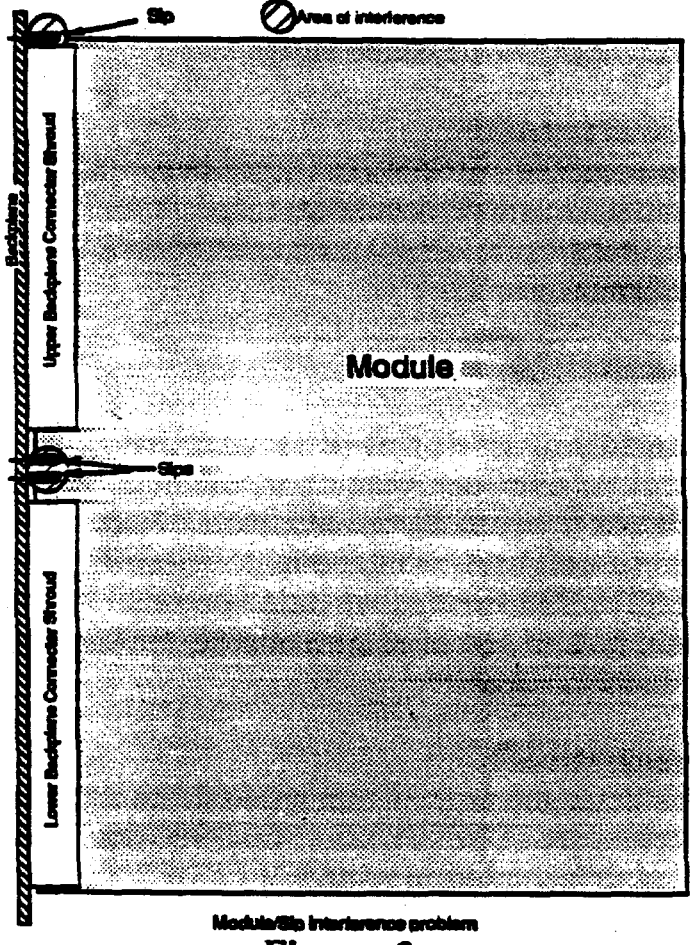

Figure 3

3. Power Distribution

3.1. Auxiliary Backplane

3.1.1. Specification

Power and ground distribution for the Auxiliary section of the backplane is through internal power layers in the backplane. There are separate layers for +5.0 Volts @ 120 Amps, -5.2 Volts @ 120 Amps, -2.0 Volts @ 50 Amps and Ground @ 290 Amps. The 26 MHZ and 53 MHZ clocks are in an internal layer with ground planes on either side. There are no active components on the Auxiliary backplane. The power should be distributed in a way that insures a voltage drop across the backplane of less than 0.01 Volts for the ground plane and 0.030 Volts for voltage planes. Termination resistors are socketed.

The power pins will be the same for all Auxiliary cards except the Sequencer module slot 13 and slot 0 which has none. The large number of pins required on some modules means it won't be possible to arrange the power pins a per IEEE 960. There is a limit of 3 amps per Auxiliary card (except the Sequencer slot Auxiliary card) for all supplies.

3.1.2. Test Procedure

As the power requirement for the Auxiliary backplane is significantly less than the Segment backplane no special tests are required if the crate passes the test at the Segment backplane. A simple check will be made of the voltage drops at the Auxiliary connector.

3.1.3. Test Result

3.1.4. Additional Power Bus Required for Postamp/Comp.

There is the possibility of using existing contacts on the FASTBUS crate segment connector for bringing the plus and minus 3.5 volt power supply voltages to the Postamp/Comparator modules. These voltages are required for some of the ASIC's used on this module. In order to determine the feasibility of this idea, a series of measurements should be conducted on a typical crate used in the SSD project.

3.1.4.1. Specification

The FASTBUS Crate segment pins are specified to handle a maximum of three amperes each. (See ANSI/IEEE Std 960-1986, section 13.2.1 (e)). Each P/C Module is expected to require +3.5 V @ 7.07 amperes and -3.5 V @ 3.52 amperes. Thus three pins for the +3.5 and 2 pins for the -3.5 should be adequate for each P/C Module.

There are to be twelve P/C Modules per crate requiring +3.5 V @ 12x7.07 = 85 amperes and -3.5 V @ 12x3.52 = 42 amperes per crate.

The following 8 existing busses are being considered.

1) +28 Volts (pin B02.stations 0 through 12)::[06 and 07]
2) +28 Volts (pin B02.stations 13 through 25)::[19 and 20]
3) +28 Volts (pin B03.stations 0 through 12)::[04 and 05]
4) +28 Volts (pin B03.stations 13 through 25)::[17 and 18]
5) +15 Volts (pin B04.stations 0 through 12)::[05 and 06]
6) +15 Volts (pin B04.stations 13 through 25)::[18 and 19]
7) -15 Volts (pin B05.stations 0 through 12)::[07 and 08]
8) -15 Volts (pin B05.stations 13 through 25)::[20 and 21]

The information inside the brackets "[ ]" represents station numbers between which the power supply connection to the bus exists.

In order to determine the quality of the bus, a few simple measurements should be made. In general, a current source will be connected across a portion of the bus structure, and the resulting voltages drops for various portions of the backplane bus will be recorded. The current source to be used should have an output of 2 amperes plus or minus 2 percent, an output impedance of at least 1 kΩ, and an output voltage of 1/2 volt,.plus or minus 1/4 volt. One might expect to measure between 5 and 10 millivolt drops between stations where current is flowing.

3.1.4.2. Test Procedure and Result

Instruments used:

HP 62278 Power Supply
Keithley 179A DVM

Bus 1 (Upper +28 volt bus, stations 0 through 12)

Connect one lead of the current source to pin B02 at station 0 , and the other lead to the bus connection between stations 06 and 07. Use a Digital Volt Meter (DVM) capable of measuring 0.1 millivolt changes. Connect one lead of the DVM to pin B02 at station 01,and connect the other lead to the pin B02 of the following stations and record the voltage.

Station	Millivolts
02	0.55
03	1.08
04	1.52
05	1.98
06	3.03
07	3.03
08	2.94
09	2.93

Connect one lead of the current source from pin B02 at station 12, and the other lead to the bus connection between stations 06 and 07. Connect one lead of the DVM to pin B02 at station 11, and connect the other lead to the pin B02 of the following stations and record the voltage.

Station	Millivolts
02	0.49
03	0.96
04	1.46
05	2.10
06	2.46
07	2.29
08	2.27
09	2.28

Bus 2 (Upper +28 volt bus, stations 13 through 25)
Connect one lead of the current source from pin B02 at station 13, and the other lead to the bus connection between stations 19 and 20. Connect one lead of the DVM to pin B02 at station 14. Connect the other lead to the pin B02 of the following stations and record the voltage.

Station	Millivolts
02	0.51
03	0.99
04	1.45
05	1.88
06	2.87
07	2.89
08	2.82
09	2.82

Connect one lead of the current source from pin B02 at station 25, and the other lead to the bus connection between stations 19 and 20. Connect one lead of the DVM to pin B02 at station 24. Connect the other lead to the pin B02 of the following stations and record the voltage.

Station	Millivolts
02	0.56
03	1.09
04	1.56
05	2.24
06	2.58
07	2.43
08	2.43
09	2.43

Bus 3 (Lower +28 volt bus, stations 0 through 12)
Connect one lead of the current source to pin B03 at station 0 , and the other lead to the bus connection between stations 04 and 05. Connect one lead of the DVM to pin B03 at station 01,and connect the other lead to the pin B03 of the following stations and record the voltage.

Station	Millivolts
02	0.70
03	1.43
04	2.19
05	2.31
06	2.31
07	2.31
08	2.31
09	2.32

Connect one lead of the current source from pin B03 at station 12, and the other lead to the bus connection between stations 04 and 05. Connect one lead of the DVM to pin B03 at station 11, and connect the other lead to the pin B03 of the following stations and record the voltage.

Station	Millivolts
02	0.75
03	1.50
04	2.24
05	2.31
06	4.27
07	5.27
08	5.81
09	5.78

Bus 4 (Lower +28 volt bus, stations 13 through 25)
Connect one lead of the current source from pin B03 at station 13, and the other lead to the bus connection between stations 17 and 18. Connect one lead of the DVM to pin B03 at station 14. Connect the other lead to the pin B03 of the following stations and record the voltage.

Station	Millivolts
02	0.77
03	1.53
04	2.34
05	2.47
06	2.46
07	2.46
08	2.46
09	2.47

Connect one lead of the current source from pin B03 at station 25, and the other lead to the bus connection between stations 17 and 18. Connect one lead of the DVM to pin B03 at station 24. Connect the other lead to the pin B03 of the following stations and record the voltage.

Station	Millivolts
02	0.78
03	1.56
04	2.32
05	3.41
06	4.41
07	5.44
08	5.99
09	5.97

Bus 5 (+15 volts, stations 0 through 12)

Connect one lead of the current source to pin B04 at station 0 , and the other lead to the bus connection between stations 05 and 06. Connect one lead of the DVM to pin B04 at station 01,and connect the other lead to the pin B04 of the following stations and record the voltage.

Station	Millivolts
02	0.20
03	0.39
04	0.55
05	0.86
06	0.85
07	0.73
08	0.69
09	0.67

Connect one lead of the current source from pin B04 at station 12, and the other lead to the bus connection between stations 05 and 06. Connect one lead of the DVM to pin B04 at station 11, and connect the other lead to the pin B04 of the following stations and record the voltage.

Station	Millivolts
02	0.20
03	0.38
04	0.51
05	0.74
06	0.98
07	1.09
08	0.95
09	0.92

Bus 6 (+15 volts, stations 13 through 25)
Connect one lead of the current source from pin B04 at station 13, and the other lead to the bus connection between stations 18 and 19. Connect one lead of the DVM to pin B04 at station 14. Connect the other lead to the pin B04 of the following stations and record the voltage.

Station	Millivolts
02	0.21
03	0.40
04	0.56
05	0.86
06	0.84
07	0.74
08	0.69
09	0.68

Connect one lead of the current source from pin B04 at station 25, and the other lead to the bus connection between stations 18 and 19. Connect one lead of the DVM to pin B04 at station 24. Connect the other lead to the pin B04 of the following stations and record the voltage.

Station	Millivolts
02	0.21
03	0.39
04	0.53
05	0.78
06	1.03
07	1.13
08	0.98
09	0.94

Bus 7 (-15 volts, stations 0 through 12)

Connect one lead of the current source to pin B05 at station 0 , and the other lead to the bus connection between stations 07 and 08. Connect one lead of the DVM to pin B05 at station 01,and connect the other lead to the pin B05 of the following stations and record the voltage.

Station	Millivolts
02	0.33
03	0.56
04	0.75
05	0.93
06	1.21
07	1.73
08	1.53
09	1.33

Connect one lead of the current source from pin B05 at station 12, and the other lead to the bus connection between stations 07 and 08. Connect one lead of the DVM to pin B05 at station 11, and connect the other lead to the pin B05 of the following stations and record the voltage.

Station	Millivolts
02	0.38
03	0.68
04	1.05
05	1.40
06	1.05
07	0.94
08	0.90
09	0.88

Bus 8 (-15 volts, stations 13 through 25)

Connect one lead of the current source from pin B05 at station 13, and the other lead to the bus connection between stations 20 and 21. Connect one lead of the DVM to pin B05 at station 14. Connect the other lead to the pin B05 of the following stations and record the voltage.

Station	Millivolts
02	0.34
03	0.57
04	0.75
05	0.96
06	1.24
07	1.75
08	1.54
09	1.35

Connect one lead of the current source from pin B05 at station 25, and the other lead to the bus connection between stations 20 and 21. Connect one lead of the DVM to pin B05 at station 24. Connect the other lead to the pin B05 of the following stations and record the voltage.

Station	Millivolts
02	0.38
03	0.69
04	1.08
05	1.43
06	1.08
07	0.97
08	0.93
09	0.91

3.2. Segment Backplane

3.2.1. Specification

The Segment backplane power distribution will be as specified in IEEE 960, Chapters 14 and 15.

3.2.2. Test Procedure

A prototype crate was tested at Kinetic Systems Inc. for evaluation on a specially built FASTBUS crate power test stand. The test stand consists of a small rack and Kinetic Systems standard FASTBUS power supply. A shunt is provided to be inserted in the power leads to allow measurement of total current for a given supply voltage. Special load modules composed of FASTBUS cards with dip and sip terminators across the boards are used to load the crate. These load modules are designed to allow use with -5.2 Volts, +5.0 Volts and -2.0 Volts. The modules can be used with only one voltage at a time, this is accomplished through the use of jumper wires along the edges of the modules. These modules thus provide a uniform current load throughout the crate for one supply voltage at a time.

The test procedure is to fill the crate with test modules jumpered for one of the supply voltages and measure the voltage drop from the power bus to the pins at the top and bottom of each slot. This yeilds only the differential voltage across the backplane. Each voltage is tested in turn.

3.2.3. Test Result

Test results for crate serial #0553 are shown in tables below:

-5.2 Volt bus

Bus to Ground voltage -4.22 V (supplies current limited @ 320 Amperes.)
Current 320 Amps. (measured with 50 mv/500 Ampere shunt)
Measured at the top and bottom of the crate segment connector, all values are in millivolts.

Slot #	0	3	5	7	11	15	17	19	20	21	22	23	24	25
Top	33	33	33	33	33	34	34	35	35	36	36	37	37	37
Bot.	23	21	20	20	20	20	21	22	23	25	27	30	31	32

+5 Volt bus

Bus to Ground voltage +4.61 V (supplies current limited @ 340 Amperes.)
Current 340 Amps. (measured with 50 mv/500 Ampere shunt)
Measured at the top and bottom of the crate segment connector, all values are in millivolts.

Slot #	0	3	5	7	11	15	17	19	20	21	22	23	24	25
Top	31	31	29	29	28	27		27				28		29
Bot.	25	24	18	17	15	14		15				20		24

-2 Volt bus

Bus to Ground voltage -2.0 V
Current 140 Amps. (measured with 50 mv/500 Ampere shunt)
Measured at the top and bottom of the crate segment connector, all values are in millivolts.

Slot #	0	3	5	7	11	15	17	19	20	21	22	23	24	25
Top	24		23	23	22	22		22			23			23
Bot.	17	15	13	12	12	11		11			12			14

The maximum voltage difference across the backplane is specified as 30 mv when fully loaded. The maximum measured was 17 mv.

4. Signal Layers

Signals for each layer are isolated due to the power planes inserted in the multilayer card. This should reduce crosstalk for data lines and prevent the clock from being coupled to other signals. Each group of signals is discussed separately below. All terminations and drivers will be on daughter cards except the 26 MHZ clock bus, Reset bus, Sync bus, Sync Err bus and Event Address Data and Strobe lines which are terminated on the backplane. Terminations are single except as noted.

All pinouts are specified in Appendix A. Slot 0 (rightmost slot viewed from front of crate) has no connections in the Auxiliary backplane. A Netlist can be supplied in any of several computer formats.

5. Electrical

5.1. Specification

All signals conform to ECL standard levels and terminations. **Impedance of transmission lines shall be specified when fully loaded by connectors and a one inch stub with a single ECL receiver on each daughter card which receives that signal.** Termination resistance not less than 25 Ohms for double terminated bus lines (10 Event Address, 2 Sync, 1 Reset) and 50 Ohms for single terminated lines. Impedance not exceeding 100 Ohms. Variation of impedance shall not be greater than 10%.

5.2. Test Procedure

Impedance will be measured using a Time Domain Reflectometer (TDR) with a resolution of at least 1 inch. The impedance will be measured without terminations in place and the TDR connected in place of the drivers. Measurements will be taken for both the loaded and unloaded condition. Loads will be simulated by attaching capacitors of appropriate size to the backplane pins. Figure 4 is a diagram of the test setup. Table 1 shows the test results.

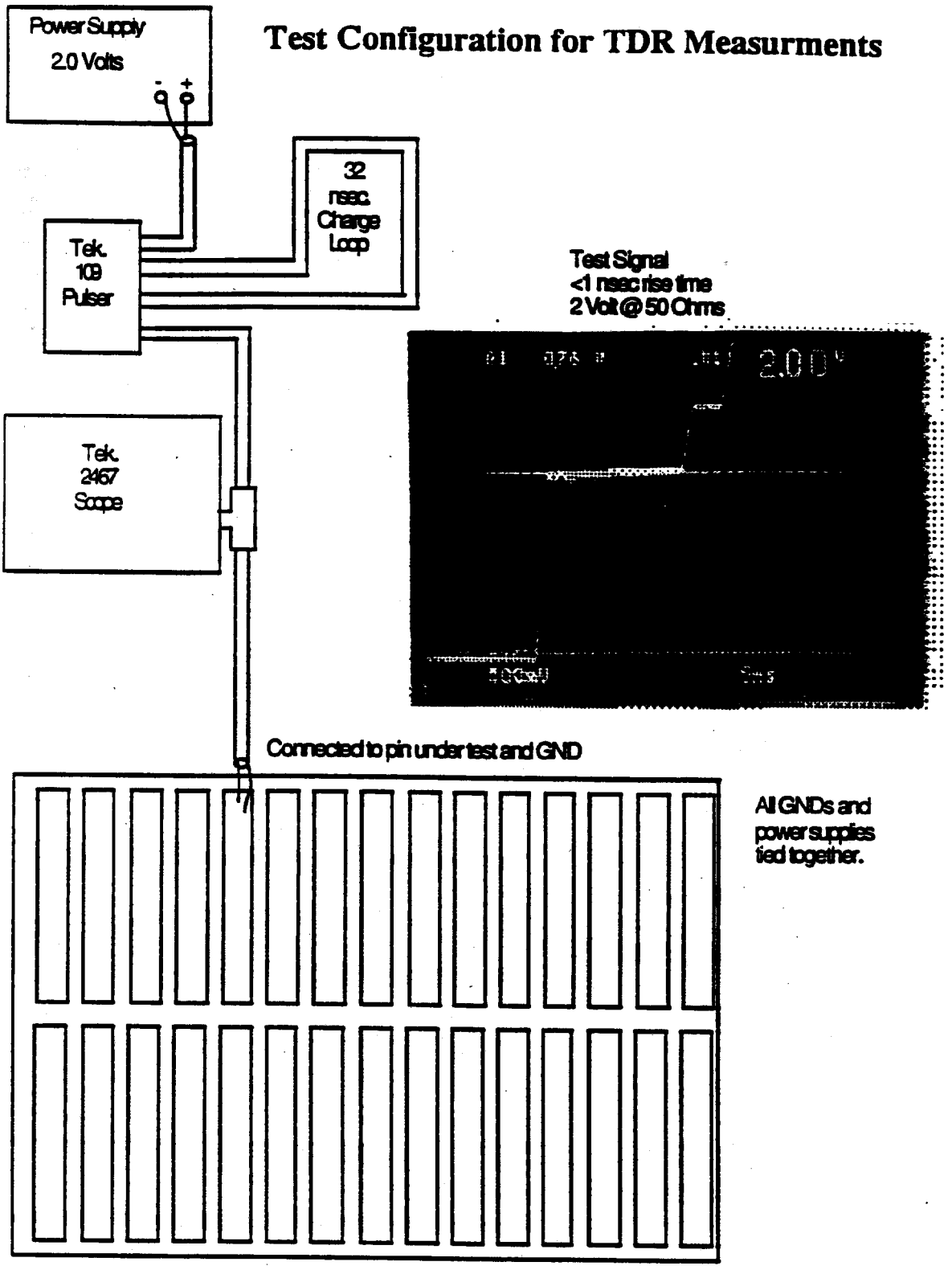
Test Configuration for TDR Measurments
Power Supply
2.0 Volts
-
+
32
nsec.
Charge
Loop
Tek.
109
Pulser
Tek.
2467
Scope
Test Signal
<1 nsec rise time
2 Volt @ 50 Ohms
2.00
Connected to pin under test and GND
All GNDs and
power supplies
tied together.

Figure 4

TDR Measurements (Unloaded Lines)

2/14/1990 #550

	ρ	Zo	Zo'	Ei	Er	% Error	Calc. Imped	Meas. Delay	Calc. Delay
	(Er-Ei)/Ei	Ohms	Ohms	Volts	Volts		Ohms	Nanosecs (Delay*2)	Nanosecs (Loaded)
	75 Ohm line measurement for calibration								
	0.23	50	80	2.00	2.46	6.5	75.0	-	-
	Ideal 75 Ohm Measurements								
Note 1	0.20	50	75	2.00	2.40	0.0	75.0	-	-
Note 2		50	75	2.00	2.40				
	53 Mhz Clock Lines								
Note 1	0.38	50	110	2.00	2.75	25.4	87.7	4.4	1.5
Note 2		50	110	2.00	2.75				
Note 4	0.31	50	94	2.00	2.61	7.1	87.7	4.4	1.5
Note 3	**Reset Line(1-B8)**								
Note 1	0.00	50	50	2.00	2.00	-51.5	103.0	10.9	4.0
Note 2		50	50	2.00	2.00				
	Hit Data 0(13-C3)								
Note 1	0.21	50	76	2.00	2.41	17.7	64.4	4.4	1.8
	Hit Data 0(13-A3)								
Note 1	0.21	50	76	2.00	2.41	17.7	64.4	4.4	1.8
Note 3	**26 Mhz Clock(13-C33)**								
Note 1	0.12	50	63	2.00	2.23	-38.8	103.0	5.4	2.3
Note 3	**26 Mhz Clock(13-A33)**								
Note 1	0.12	50	63	2.00	2.23	-38.8	103.0	5.4	2.3
Note 3	**Sync(1-C9)**								
Note 1	0.09	50	59	2.00	2.17	-42.4	103.0	9.0	4.6
Note 3	**Sync Error(1-C10)**								
Note 1	0.09	50	59	2.00	2.17	-42.4	103.0	9.0	4.6
Note 3	**Data Valid(13-C11)**								
Note 1	0.24	50	81	2.00	2.47	25.3	64.4		4.6
Note 3	**AD Lines(25-A22)**								
Note 1	0.00	50	50	2.00	2.00	-22.4	64.4		4.6

Note 1 1st Formula: Zo'=(1+((Er-Ei)/Ei))/(1-((Er-Ei)/Ei))*Zo

Note 2 2nd Formula: Zo'=((Zo*Er)+(Zo*Ei))/(Ei-Er)

Note 3 These lines are Partialy Loaded as they are bussed and have connectors installed.

Note 4 Crate #553

Table 1

The Measured impedance of lines in the backplane is consistently high. The calculations are based on the manufacturers layup and specification of .010 inch trace width, the dielectric constant is assumed to be 4.7 based on industry practice for fiber-glass laminate material.

The parameters most likely to case the observed discrepancy are trace width and dielectric constant. A 50% reduction in trace width to .005 inch would cause the observed error as would a dielectric constant of 3.

To test the trace width the 53 Mhz clock lines were calculated to be .176 Ohm for the given copper thickness and width. A clock line was measured to be .4 Ohm. This is consistent with the error we have observed. See Table 4 for data.

The capacitance of a 53 Mhz clock line was measured to be 20 pf for 7.95 inches of line, or 30 pf/foot. The geometries given by the manufacturer should yield a capacitance of approximately 27 pf/foot (from table 3-10 on page 47 of the MECL System design Handbook) and a .005 inch line width would be 25 pf/foot. The difference is within the measurement and construction tolerance.

An attempt was made to measure the dielectric constant by using the identical layers 2 and 3 which have matching areas and are solid copper.

Dielectric Constant Measurement

Formula: Er = (C x 10**12 x t) / 8.85 A

Er is the relative Dielectric Constant

C is the capacitance in Farads

t is the dielectric thickness in meters

A is the area of one plate in square meters

	Er	C	Layers 2 & 3 Mult.	t	Constant	A
Crate #550	5.73529473	36900.E-12	1.00E+12	.20320E-03	8.85	0.147724
Crate #553	5.81300875	37400.E-12	1.00E+12	.20320E-03	8.85	0.147724

5.3. Segment Backplane

5.3.1. Connectivity

5.3.1.1. Specification

Connectivity as specified in IEEE 960, Chapter 14, no special modifications.

5.3.1.2. Test Procedure

The Computing Division, Instrument Repair Group will test connectivity with a special FASTBUS crate test stand. This procedure is documented in PN 383, "Diagnostic Test for FASTBUS Crate Backplanes", which is obtainable from the Instrument Repair Group of the Fermilab Computing Department.

5.3.1.3. Test Result

The measurements taken by Instrument Repair were checked by hand and all connections were found to be correct. There was some misunderstanding about the power supplies which caused the results shown in Table 3 and Table 4. These tables are from the Instrument Repair test facility.

Summary fo rate 1 Ø553 09-MAR-89 Fastbus crat est V1.0

Slot Written	Slot Read	Pin Written	Pin Open	Pin Shorted
2	1	B 63	B 14	
2	1	B 63	B 15	
2	1	B 63	B 22	
2	1	B 63	B 32	
2	1	B 63	B 63	
2	1	B 63	B 64	
10	9	B 63	B 14	
10	9	B 63	B 15	
10	9	B 63	B 22	
10	9	B 63	B 32	
10	9	B 63	B 63	
10	9	B 63	B 64	
10	11	B 63	B 14	
10	11	B 63	B 15	
10	11	B 63	B 22	
10	11	B 63	B 32	
10	11	B 63	B 63	
10	11	B 63	B 64	
12	13	B 4	B 4	
12	13	B 5	B 5	
12	13	B 6	B 6	

Total errors detected = 21

Table 3

Summary for Crate # Ø550 09-MAR-89 Fastbus Crate Test V1.0

Slot Written	Slot Read	Pin Written	Pin Open	Pin Shorted
0	1	B 38	B 38	
2	1	B 63	B 14	
2	1	B 63	B 15	
2	1	B 63	B 22	
2	1	B 63	B 52	
2	1	B 63	B 63	
2	1	B 63	B 64	
12	13	B 4	B 4	
12	13	B 5	B 5	
12	13	B 6	B 6	
24	25	B 63	B 14	
24	25	B 63	B 15	
24	25	B 63	B 22	
24	25	B 63	B 52	
24	25	B 63	B 63	
24	25	B 63	B 64	

Total errors detected = 15

Brian Anderson

Table 4

5.3.2. Impedance

5.3.2.1. Specification

Impedance is as specified in IEEE 960, Chapter 14, there are no special modifications.

5.3.2.2. Test Procedure

Impedance of the Segment backplane will be tested as described in section 5.2 with the exception that actual modules will be installed to provide a load.

5.3.2.3. Test Result

The Impedance of the Segment backplane was measured to be 50 Ohms with the connector pins installed but not loaded with modules. See Table 1.

5.4. Auxiliary Backplane

5.4.1. 53 MHZ Clock

5.4.1.1. Specification

The 53 MHZ clock has the special requirement that it must be distributed with a very small skew to the Post Amp/Comp. modules and to the Encoder modules. The specification given is +/- 250 picoseconds. It is possible to match the distribution line length for 24 modules (Post Amp & Encoder) but receivers and drivers must be kept to a minimum as the typical skew of ECL 10KH is 800 picoseconds min. to max. per IC. There are two 53 MHZ clocks labeled phase 1 and phase 2. The phase 1 clock goes to the Post Amp/Comp. boards and the phase 2 clock to the Encoder boards. A MC10E111 clock driver is used. as shown in the circuit of Figure 5, the skew for this part is specified as 100 picoseconds min. to max.

The Skew is then 100 picoseconds for the MC10E111 plus the skew variation of the backplane. The backplane lines must be matched to 150 picoseconds delay. As the driver and loads affect the skew, all lines on daughter cards must be less than 1 inch and only one load per Post Amp or Encoder.

The clock is driven from the Sequence in slot 13 of the FASTBUS crate. The top two pins and the bottom two pins on the outside rows of the three row connector will be used to drive the series terminations which are located as close as possible to the connector. All striplines are made as close as possible to the same propagation delay.

The stripline impedance is calculated from the equation on page 42 of the MECL System Design Handbook as follows;

Zo (Stripline)	Er (Dielectric)	b (Thickness)	t (Copper)	w (Strip Width)
85 Ohms	5	100 mills	0.003 mills	10 mills

A correction must be made as shown by the equation on page 152 to allow for loading. This is the line capacitance plus connector and gate capacitance. A connector load of 7 picofarads (2.2 for pins, 2 for a stub and 2.8 connectors) and a gate load of 3 picofarads (page 141) was assumed. The line capacitance is from the equation on page 142.

Zo' (Stripline)	CT	Co	Cg	Ccon
51 Ohms	10pf	2.2 pf/inch	3pf	7pf

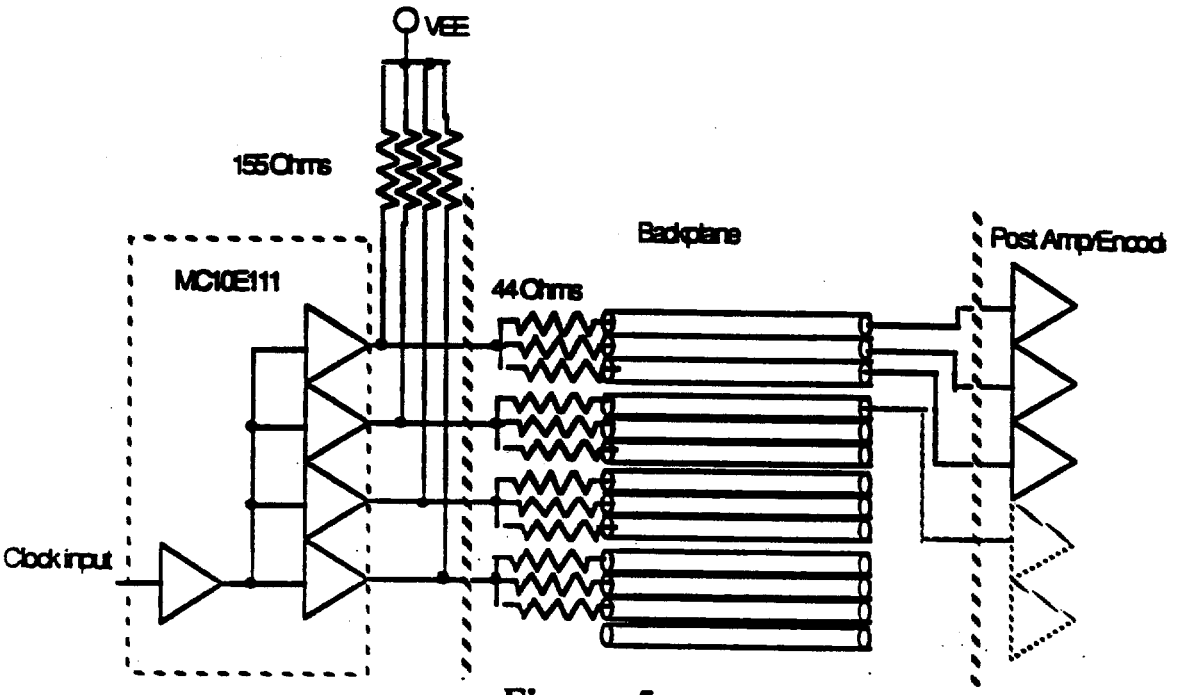

Figure 5

The series resistor value is given by subtracting the nominal output impedance for MECL 10K of 7 Ohms (page 46) from Zo', thus Rs = 44 Ohms.
The value of the emitter pulldown resistor is from the formula on page 48. This yields the maximum pulldown resistor which may be used for a given fanout and Zo'. The minimum value is determined by the maximum output current. The maximum current for ECL 10K is 50 ma and the recommended value is 25 ma.

RE(Max)	Zo'	Rs	n (fanout)	Isource
155	51 Ohms	44 Ohms	3	28ma

The clock will be received by the Post Amp module on the top left pin (C01) and the fourth from bottom left (C62) on the Encoder modules (viewed from the front of the crate).

5.4.1.2. Connectivity

Connectivity is checked by comparing Ohm meter readings of appropriate pins against schematic above and pin-out list. All signals are correctly connected.

5.4.1.3. Impedance

Impedance of the 53 Mhz Clock lines were tested as described in section 5.2. See Table 1 for unloaded Impedance. Resistence measurements were made to try to determine the cause of the impedance error. The resistence was measured using a known current through the line under test and measuring the voltage drop. Ohms law was then used to calculate the resistence. A check was done by using a sensitive Ohmmeter, the results agreed with the current method. See Table 4 for resistence results and section 5.2 and Table 1 for impedance tests.

R of 53 MHZ Lines

A	V	R		
			Crate #550	
1.200	.55	.458		SH25-C1
1.204	.55	.457		23-C1
1.195	.55	.460		21-C1
1.215	.55	.453		17-C1
1.205	.55	.456		13-C1
1.182	.55	.465		15-C1
1.145	.56	.489		12-C1
1.201	.55	.458		10-C1
1.160	.55	.466		8-C1
1.161	.56	.482		6-C1
1.190	.55	.462		4-C1
1.190	.55	.462		2-C1
1.114	.55	.494		1 C62
1.127	.55	.447		3 C62
1.230	.53	.430	Crate # 553	24-C62
1.250	.52	.416		20-C62
1.188	.51	.432		1 C62
1.181	.51	.432		3 C62

Table 4

5.4.2. 26 MHZ Clock

5.4.2.1. Specification

The 26 MHZ clock is bussed to all Encoder slots (12) and is driven from the center by the sequencer card with two MC10123 bus drivers. The drivers will be on the Sequencer, the bus is terminated at each end of the backplane with a resistor to -2.0 Volts. These are driven independently and are single terminated.

The left (C33) and right (A33) connector pins are used to drive the clock busses. The Encoder modules receive the clock on pin C49 (crate viewed from the front) of the Auxiliary connector.

All drivers and receivers are on modules and lead lengths must be less than 1 inch.

5.4.2.2. Connectivity

Connectivity is checked by comparing Ohm meter readings of appropriate pins against pin-out list. Connectivity is correct.

5.4.2.3. Impedance

Impedance of the Segment backplane will be tested as described in section 5.2 with the exception that actual modules will be installed to provide a load. See Table 1 for unloaded impedance.

5.4.3. Post Amp Data

5.4.3.1. Specification

There are 128 data channels transmitted from the Post Amp to the Encoder module. The modules are always adjacent and line lengths including connectors must be less than 2 inches.

As the 128 channels will require two rows of pins (65 pins/row), the adjacent rows of the connectors for the Post Amp and Encoder modules are used for I/O. This leaves one row of Encoder module pins for communication with the Sequencer module. The Auxiliary card signals are picked from the same pins used for signals transmitted to the encoder. This means one Auxiliary card will pick off row B on the Encoder, which is connected to row A on the Post Amp and the other will Pick up row B directly from the Post Amp module. See Figure 6.

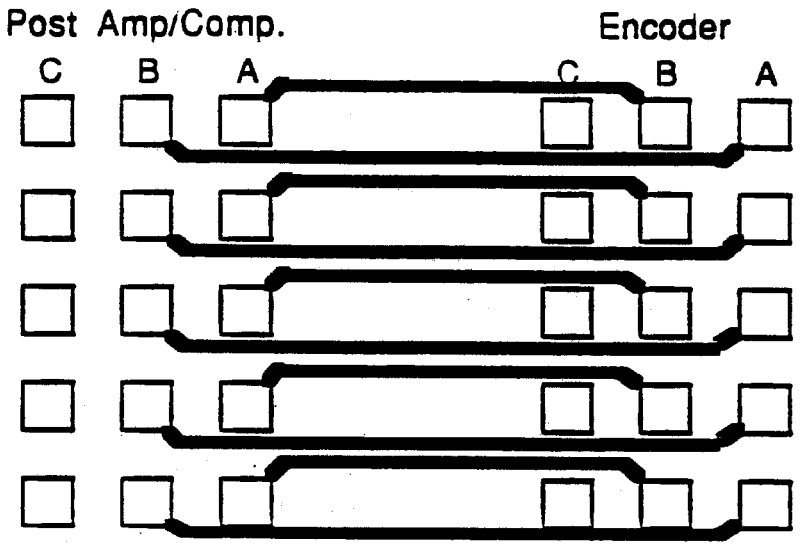

Figure 6

There are 16 analog and 16 digital sums which must be transmitted by the Auxiliary cards to the trigger logic. These are connected using a similar scheme which allows the Auxiliary cards to be identical for Post Amp and Encoder slots. See Figure 7.

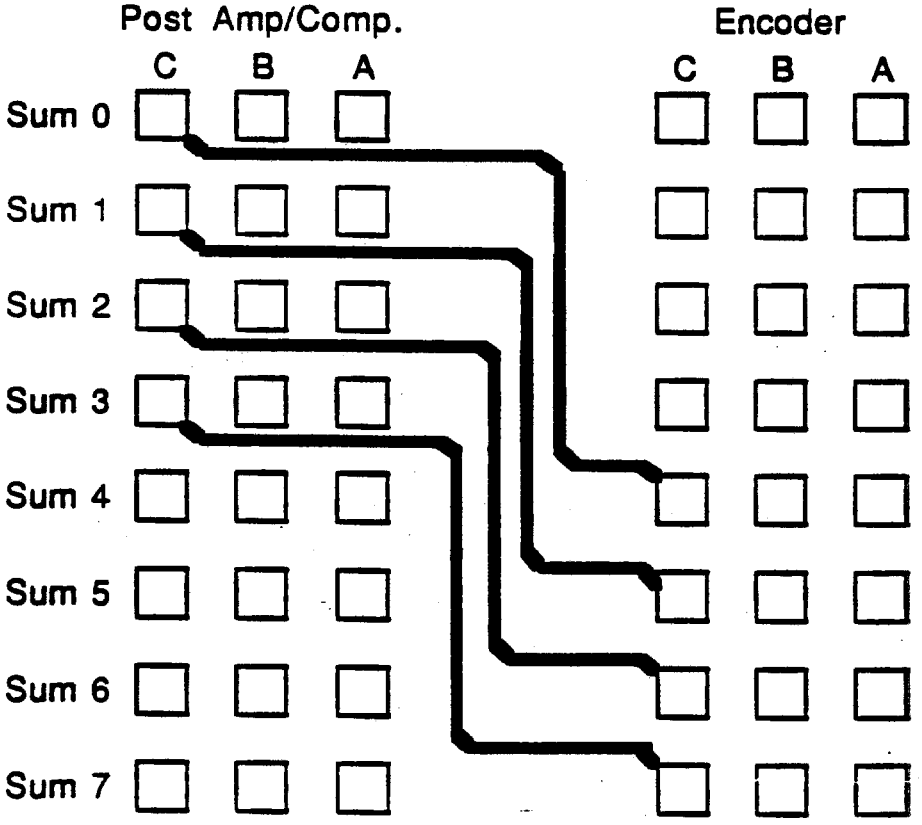

Figure 7

5.4.3.2. Connectivity

Connectivity is checked by comparing Ohm meter readings of appropriate pins against schematic above and pin-out list. Connectivity is as specified.

5.4.3.3. Impedance

Impedance of the Segment backplane will be tested as described in section 5.2. See Table 1 for unloaded impedance.

5.4.4. Hit Data

5.4.4.1. Specification

There are eight Hit Data lines and one Data Valid for each Encoder module. These are connected from row C pins not used by the Post Amp data lines, to the Sequencer card.

5.4.4.2. Connectivity

Connectivity is checked by comparing Ohm meter readings of appropriate pins against schematic above and pin-out list. All signals are correctly connected.

5.4.4.3. Impedance

Impedance of the Segment backplane will be tested as described in section 5.2. See Table 1 for unloaded impedance.

5.4.5. Event Address

5.4.5.1. Specification

The Event Address lines are bussed in the outer layers of the board. There are eight data bits, Event Address Enable and one Event Address Strobe line. Because these lines are bussed to the 12 Encoder slots, the effect of capacitive loading on impedance must be considered as the load is distributed over eight inches of backplane. These lines are terminated at each end of the backplane with a resistor to -2.0 Volts. They are driven from the Sequencer module and terminated at the last backplane connectors. The lines on the Encoder cards are stubs off this bus and must be kept to less than one inch.

5.4.5.2. Connectivity

Connectivity is checked by comparing Ohm meter readings of appropriate pins against schematic above and pin-out list. Connectivity is as specified.

5.4.5.3. Impedance

Impedance of the Segment backplane will be tested as described in section 5.2. See Table 1 for unloaded impedance.

5.4.6. Reset and Sync

5.4.6.1. Specification

The Reset is bussed to all slots except slot 0. The two Sync lines are bussed to all Encoder card slots. These lines are driven from the Sequencer module pins B01, B10 and B09, and are terminated at each end of the backplane with a resistor to -2.0 Volts. The Reset signals are connected to all Post Amp and Encoder cards. The Traces on the daughter cards are stubs off this bus and must be kept to less than one inch.

5.4.6.2. Connectivity

Connectivity is checked by comparing Ohm meter readings of appropriate pins against schematic above and pin-out list. Connectivity is correct.

5.4.6.3. Impedance

Impedance of the Segment backplane will be tested as described in section 5.2. See Table 1 for unloaded impedance.